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Causal Discovery in Electronic Circuits and Its Application in Fault Diagnosis

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Abstract— **This article demonstrates that causal discovery approaches can be applied to analog electronic circuits made of Bipolar Junction Transistors (BJTs) to find out the causal relationships among different variables of the circuit. Moreover, the obtained causal relationship structure in the form of a Directed Acyclic Graph (DAG), can be used for diagnosis and analysis of such circuits. First, it is shown that the operation process of a transistor has an inherent notion of causality, which is then exploited to show that the various parameters of a BJT circuit can be expressed in the form of Structural Equation Models (SEM). The results demonstrated using data generated using LTspice establishes that the causal structure of a BJT circuit can be retrieved using data driven causal discovery algorithms. This opens new horizons for analysis and diagnosis of BJT circuits. An example case study of circuit diagnosis is presented to showcase the capability and efficiency of the proposed method.**

I. INTRODUCTION

Modern integrated circuits (IC) comprise of a copious and ever increasing number of components which makes the diagnosis of such circuits a challenging task. Moreover, the diagnosis of analog ICs is considerably more complicated and challenging compared to its digital counter part [1]. In literature many different methods are proposed over the years to perform circuit diagnosis [1], [2]. These methods are primarily classified into two categories, namely; Simulation Before Test (SBT) and Simulation After Test (SAT) [1].

SBT methods employ a large number of simulated fault scenarios where the data generated is compiled to create a fault library or a statistical database. Such databases are used as a look up table against the actual test data to detect faults. Some traditional SBT approaches include model based identification [3] that utilizes mathematical model of system and fault data, hierarchical method [4] that partitions the circuit and then builds a hierarchy, and others use signal analysis based approaches [5]. Few modern approaches of SBT includes meta-heuristic optimization based approach, such as, particle swarm optimization [6] and genetic algorithm (GE) [7] based methods, machine learning based approach [8], and hybrid approach [9] that combines meta-heuristic and machine learning methods. In case of SBT approach, even though, once the fault dictionary is built the detection of commonly occurring faults becomes an easier task, the process of building the fault dictionaries and databases requires a large amount of data and complex computations.

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SAT methods perform simulation of the circuit after test data is obtained. The fault diagnosis problem is modeled via non-linear equations whose parameters are identified using the computed test data [1]. Some of these methods include formulation of self-testing and component connection models [10] where the authors repeatedly partition the subsystems in two combinations and then test to see which combinations produce reliable and which ones produce unreliable data. After enough number of iterations the fault decision is made. More modern SAT approaches include support vector machines (SVM) [11] where SVMs are used to identify non-linear relationships among fault indicator measurement data, GE based approach [12] where the authors estimate parameters using measurement data from circuit, and functional mapping based method [13] which uses a non-linear regression model to approximate the functional relationship between parameters. Compared to the SBT methods, the SAT methods are less resource consuming but the computational complexity, memory requirement, number of required tests/measurements are still a concern as the circuit under test scales up in component counts.

The contributions of this article are two fold: 1) Firstly, it is shown that BJTs are causal devices and data generated from a BJT circuit can be used to perform causal search and identify causal relationships among the variables of the circuit and thus reconstruct the underlying topology. 2) Secondly, it is experimentally shown that the identified topology/structure of the network can alleviate the process of fault diagnosis. The proposed causal graph based diagnosis technique can alleviate the problem of computational complexity and memory requirement, and can minimize the number of test required to identify faults.

The article is organized as follows. In Section II some useful notions of graph theory and causal inference are described. Section III establishes the causal relations in BJT operation which is then used in Section IV to show that equations of a BJT circuit can be posed as SEM. Section V demonstrates the construction of representative causal graph of a BJT circuit using simulation data. Section V also presents a simple fault diagnosis technique using the constructed graph. Finally, Section VI concludes the article and makes comments on future works.

II. SOME BASIC NOTIONS OF GRAPH THEORY AND CAUSAL INFERENCE

This section presents a few notions of graph theory and causal inference [14], [15] that are used in this paper. First,

some basic definitions of graph theory are presented then some useful notions of causal inference are described.

Definition 1: (Directed, Undirected, and Partially Directed Graph): A graph $G := (V,E)$, where, V is a set of nodes and E is the set of edges, is called a directed graph if each element of E is an ordered pair $(i,j) \in V \times V$ i.e. $E \subseteq \{(i,j)\} \forall i,j \in V$. If all the elements of E are unordered then G is called an undirected graph, i.e. $E \subseteq \{\{i,j\}\} \forall i,j \in V$. And if some of the edges of a graph is oriented and others are unoriented then the graph is called a partially directed graph i.e. $E \subseteq \{(i,j),\{i,j\}\} \forall i,j \in V$. Note that, we denote the directed edge $i \to j$ by (i,j), and the undirected edge $i - j$ by $\{i,j\}$.

Definition 2 (Skeleton): The skeleton of a directed graph $G = (V,E)$, is obtained by removing the orientation of the edges in E, and the skeleton is denoted by $\overline{G} = (V,\overline{E})$.

Definition 3 (Chain): Given a directed graph G, a chain from node i to j is a sequence of vertices $\{\pi_k\}_{k=1}^{n}$, such that, $(\pi_l, \pi_{l+1}) \in E$ holds $\forall 1 \leq l \leq n$, where, $\pi_1 = i$ and $\pi_n = j$.

Definition 4 (Cycle): In a directed graph G, a cycle is a chain from a node i to i itself.

Definition 5 (Path): Given a graph G, a path from node i to j is a sequence of vertices $\{\pi_k\}_{k=1}^{n}$, such that, either $(\pi_l, \pi_{l+1}) \in E$ or $(\pi_{l+1}, \pi_l) \in E$ or $\{\pi_{l+1}, \pi_l\} \in E$ holds $\forall 1 \leq l \leq n$, where, $\pi_1 = i$ and $\pi_n = j$.

Definition 6 (Directed Acyclic Graph): A directed graph G with finite number of nodes and no cycles is called a directed acyclic graph (DAG).

Definition 7 (Parent and Child): Given a directed graph G, node i is called a parent node of j if $(i,j) \in E$, and in that case j is called a child of i.

Definition 8 (Ancestor and Descendant): In a directed graph G, node i is called an ancestor of j if there is a directed chain from i to j, and in that case j is called a descendant of i. The symbolic representations $an(x)$ and $de(x)$ denotes the set of ancestors and descendants of x respectively.

Definition 9 (Collider and Fork): Consider a directed graph G, a path has a collider at node π_l if $(\pi_{l-1}, \pi_l) \in E$ and $(\pi_{l+1}, \pi_l) \in E$ holds. And a path has a fork at node π_l if $(\pi_l, \pi_{l-1}) \in E$ and $(\pi_l, \pi_{l+1}) \in E$ holds.

Definition 10 (Adjacent Nodes): In a graph $G = (V,E)$, two nodes x and y are said to be adjacent, if one of the following conditions satisfy, $1)(x,y) \in E$, $2)(y,x) \in E$, $3)\{x,y\} \in E$. The notation $adj(x,y)$ denotes x and y are adjacent, and $\sim adj(x,y)$ denotes x and y are not adjacent.

Definition 11 (Adjacency): Adjacency(G,x) is defined as the the set of nodes adjacent to x in the graph G.

Definition 12 (v-structure): A collider whose parents are not adjacent is called a *v-structure*.

Definition 13 (Equivalence Class): DAGs are said to be in the same equivalence class if they have the same skeleton and same v-structures.

Definition 14 (d-Separation): Given a graph $G := (V,E)$, two nodes x and y are said to be d-separated by a set $Z \subset V$ if at least one of the following holds,

1) The path contains a node $p \in Z$ which is not a collider.
2) If the path contains a collider at a node q, then neither q nor any of its descendants belong to the set Z.

The notation $dsep(x,Z,y)$ indicates that x and y are d-separated by Z. The sets $X \subset V$, $Y \subset V$, $Z \subset V$ are said to be d-separated if $dsep(x,Z,y)$ holds for every $x \in X$ and $y \in Y$.

Following are a few more important notions.

A. Structural Equation Model

As stated in [15], a structural equation model (SEM) also known as structural causal model (SCM) comprises of two sets of variables U, V and a set of functions F, where, U is the set of independent exogenous variables, and V is the set of endogenous variable whose interdependence is of interest. F is the set of functions that assigns value to each of the variables in V based on other endogenous and at least one exogenous variable.

Given an SEM we say that the variable x is a direct cause of y, if x appears as an input to the function f_y that assigns value to y. An illustrative example for better understanding is given below.

Example 1 (SEM):

$$U = \{u_1, u_2, u_3\}, V = \{x, y, z\}, F = \{f_x, f_y, f_z\} \quad (1)$$

$$x = f_x(u_1) \quad (2)$$

$$y = f_y(u_2) \quad (3)$$

$$z = f_z(x, y, u_3) \quad (4)$$

According to the SEM in (1) x, y are independent variables and, x and y are both direct causes of z.

Every SEM has a graphical representation. The nodes of the representative graph or DAG G, represent the variables in the set V, and the edges are assigned based on the set F. For example, if the function f_x contains y as an input then there is an edge from y to x. We often say "y is a direct cause of x" to mean "y is a parent of x." In Example 1, the edge set would be $E = \{(x,z),(y,z)\}$.

If there are underlying causal relationships among the variables of a data set then the interdependence of different variables can be expressed as an SEM. In such cases standard causal search algorithms can be used on the data set to unveil causal relationship among variables. One such algorithm is the Peter-Clark algorithm [16] which is described next.

B. Peter-Clark Algorithm

The PC algorithm, described in Algorithm 1 [16], can be used for causal discovery on data sets with the help of statistical independence test method. The algorithm takes a data set D, as input and produces an equivalence class of DAGs, with the variables in the data set forming the node set V of the graphs in the equivalence class.

The PC algorithm has two distinct stages. In the first stage it starts with a complete graph G and then gradually learns the underlying skeleton by systematically removing edges from G using a conditional independence test. In the sequel we have used the Fisher Z-test as the conditional independence test method, for further details on it the reader is referred to [17]. The second stage of PC algorithm

Algorithm 1 Peter-Clark Algorithm

Form a complete undirected graph $G = (V,E)$ by connecting every pair of nodes in V with an undirected edge.
Set $n = 0$.
repeat
  repeat
    Select an ordered pair of *adjacent* nodes $x,y \in V$, such that, cardinality of $Adjacency(G,x) \setminus \{y\} \geq n$.
    repeat
      Select $Z \subseteq Adjacency(G,x) \setminus \{y\}$ with cardinality n.
      if $(x \perp\!\!\!\perp y|Z)$ holds **then**
        Remove the edge between x and y in G.
        Save Z as Z_{xy}.
        break.
      end if
    until all $Z \subseteq Adjacency(G,x) \setminus \{y\}$ with cardinality n has been considered.
  until all adjacent pairs of nodes x and y with cardinality of $Adjacency(G,x) \setminus \{y\} \geq n$ has been considered.
  $n = n+1$.
until for all adjacent pairs of nodes x and y with cardinality of $Adjacency(G,x) \setminus \{y\} \leq n$.
repeat
  Choose $a,b,c \in V$, such that, $adj(a,c)$, $adj(b,c)$, but $\sim adj(a,b)$ in G.
  if $c \notin Z_{ab}$ **then**
    Designate c as a collier in the path from a to b in G.
  end if
until all triplets $a,b,c \in V$, such that, $adj(a,c)$, $adj(b,c)$, but $\sim adj(a,b)$ in G has been considered
repeat
  if $(a,b) \in E$, and $adj(b,c)$, and $\sim adj(a,c)$, and b is not a child of another node **then**
    Designate b as a parent of c
  end if
  if there is a directed path from a to b, and $\{a,b\} \in E$ **then**
    Designate a as a parent of b
  end if
until no more edges could be oriented.

reconstructs, whenever possible, the orientation of the edges. Thus, the PC algorithm produces an equivalence class of DAGs that describes some of the causal relationship among the variables in the data set.

III. CAUSALITY IN TRANSISTOR OPERATION

In this section we describe the operating principle of BJTs [18], [19] and then point out the causality in the described process. Before discussing the operation of a BJT in active region we discuss how the device reacts if a voltage bias is applied between only two terminals at a time.

Consider an npn transistor as shown in Fig. 1(a) where the base-emitter junction is forward biased but the collector terminal is open. As a result of the applied forward bias the depletion region in the base-emitter junction gets reduced

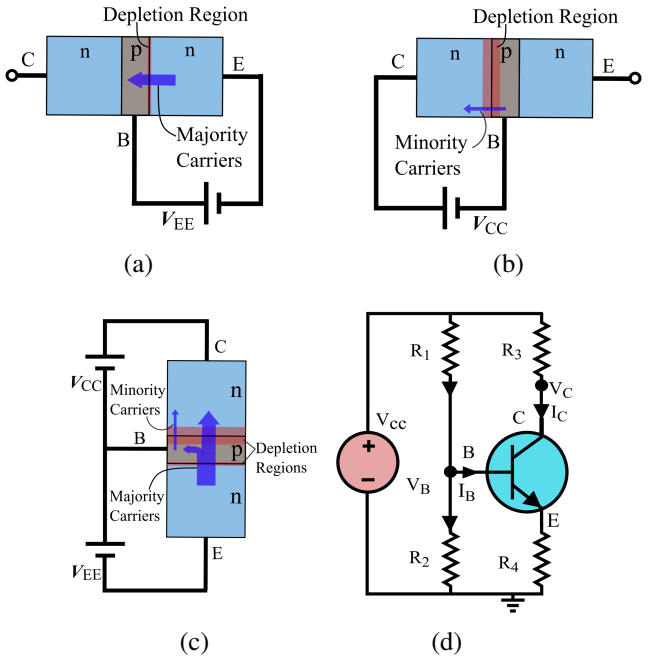

Fig. 1. (a) Carrier flow in BJT under forward biased Base-Emitter junction, (b) Carrier flow in BJT under reverse biased Base-Collector junction, (c) Carrier flow in BJT under forward biased Base-Emitter junction and reverse biased Base-Collector junction (d) Common emitter transistor in voltage divider bias configuration

and the device acts as a p-n junction diode in forward bias; as a result, a heavy flow of majority carriers from the n-type emitter to the p-type base occurs.

If the base-collector junction is reverse biased and the emitter is left open as shown in Fig. 1(b) the depletion region at the base-collector junction widens and the device acts as a reverse biased diode. Under such conditions there will be no majority carrier flow from the collector to base and a very small minority carrier flow from the base to the collector.

Now, consider an npn transistor as shown in Fig. 1(c) operating in active region i.e. the base-emitter junction is forward biased and the base-collector junction is reverse biased. Owing to the biasing conditions, the depletion region in the base-emitter junction gets very narrow where as the depletion region the the base-collector junction becomes wider. Due to the forward bias voltage applied at the base-emitter junction, a large number of majority carriers/electrons from the n-type emitter region gets injected into the base region which are then considered to be the minority carriers in the p-type base region. These injected carriers now have two paths to flow into; either into the base terminal or into the collector region. Since the sandwiched base material has a vary small width, it presents a high resistance path for the carriers to flow into the base terminal, whereas, the path from the base to the collector region presents a low resistance due to the fact that, all minority carriers in the depletion region will cross the reverse biased junction. Thus, most of the injected carriers flow into the collector region from the base. This results in a flow of current from the collector terminal to the emitter terminal. In summary, the forward

bias voltage at base-emitter terminals results in injection of majority carriers from emitter in base which further leads to the collector current flow. Thus, the collector current is a direct result of the forward bias voltage applied at the base-emitter terminals which can be considered as "*causing*" bias voltage. Although, there is a small current flow at the collector due to minority carrier flow from base to collector as shown in Fig. 1(c), this current is negligible compared to the current due to majority carriers injected from emitter.

Now that the BJT is established to have a notion of causal relationship between its input and output, one can postulate that under certain assumptions, data generated from a BJT based circuit can be leveraged to learn the underlying causal relationship among the circuit variables (currents/voltages).

Next, the equivalence of a few useful variables are established. Consider the BJT circuit in Fig. 1(d). The base and collector voltages are given by

$$V_B = \frac{R_2}{R_2 - R_1} V_{cc} - \frac{R_2 R_1}{R_2 - R_1} I_B, \tag{5}$$

$$V_C = V_{cc} - I_C R_3. \tag{6}$$

It can be observed that the base voltage V_B is a scaled and translated version of the base current I_B according to (5). Similarly, V_C is a scaled and translated version of I_C. These statements also hold true in a more complex circuit given that the load at the collector terminal is small. Hence, V_C and I_C can be considered equivalent variables representing the collector terminal from causality point of view, and same is true for V_B and I_B.

IV. STRUCTURAL EQUATION MODEL OF CASCADED BJT AMPLIFIER

This section establishes that the relationship among various voltage and currents in a cascaded direct coupled BJT amplifier can be posed as SEMs.

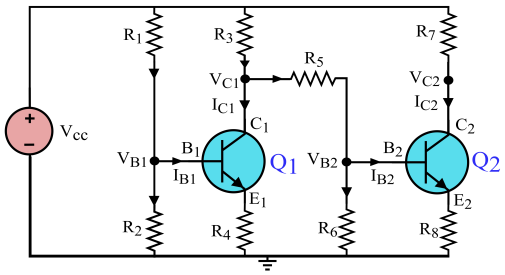

Fig. 2. Two Stage Direct Coupled BJT Amplifier

We first show that the collector current equations of the circuit shown in Fig. 2 takes the form of an SEM and then we show that the same statement holds true for the collector voltages also. In both of the cases the *temperature* of the BJTs are considered as the *exogenous* variables.

A. SEM of Collector Currents

Consider the circuit shown in Fig. 2. The collector current equations of the two transistors can be expressed as

$$I_{C1} = \beta_1 I_{B1}, \tag{7}$$

$$I_{C2} = \beta_2 \left(\frac{V_{cc} - V_{C1}}{R_3} - I_{C1} - \frac{V_{B2}}{R_6} \right), \tag{8}$$

where β_i is the current gain of the i^{th} transistor [19]. Consider I_{C1}, I_{C2} as endogenous variables, and the temperature T_1, T_2 of BJT Q_1, and Q_2 respectively as exogenous variables then the following conclusions can be drawn.

From the configuration of the circuit in Fig. 2 and physics of BJT, it can be inferred that I_{B1} only depends on T_1, and it is well known that the current gain (β) of a transistor depends on its temperature and none of the endogenous variables considered here. Which means that I_{C1} can be expressed as a function of T_1 as in (9) below:

$$I_{C1} = f_1(T_1). \tag{9}$$

I_{C1}, V_{C1} can be considered equivalent variables representing the collector from causality point of view, V_{B2} depends on I_{C1} and T_2, and V_{cc} is a constant. This implies that I_{C2} can be written as a function on I_{C1} and T_2 as in (10) below:

$$I_{C2} = f_2(I_{C1}, T_2). \tag{10}$$

Hence, we conclude that the collector current equations of the BJT circuit takes the form of an SEM.

B. SEM of Collector Voltages

The collector voltages in Fig. 2 can be expressed as in (11) and (12). Similar to the previous case, if the collector voltages, V_{C1} and V_{C2} are considered to be the endogenous variables then under certain assumptions the system equations can be expressed as an SEM as described below:

$$V_{C1} = V_{cc} - (I_{C1} + I_{B2} + I_{R6}) R_3, \tag{11}$$

$$V_{C2} = V_{cc} - \left(\frac{V_{C1} - V_{cc} + I_{C1} R_3 + \frac{V_{BE2} R_3}{R_6}}{R_3 R_8 (R_6 + \beta_2 + 1)} \right) \beta_2 R_6 R_7, \tag{12}$$

where V_{BE2} is the base to emitter voltage of transistor Q_2 which is only dependent on T_2 [18]. It is to be noted that although (11) shows the dependence of V_{C1} on I_{C1}, I_{B2}, and I_{R6}, the magnitude of I_{B2} and I_{R6} compared to I_{C1} is several orders of magnitude smaller based on the biasing conditions, which implies that effect of I_{B2}, and I_{R6} on V_{C1} can be neglected and it can be consider to be dependent only on I_{C1} which further implies that V_{C1} can be expressed as a function of T_1 as described below:

$$V_{C1} = f_3(T_1). \tag{13}$$

By similar reasoning as in case of I_{C2}, V_{C2} can be considered to be a function of V_{C1} and T_2 as in (14). Hence, the equation of V_{C2} takes the form:

$$V_{C2} = f_4(V_{C1}, T_2). \tag{14}$$

With collector current and voltage equations posed as SEMs, voltage and current measurement data from a given BJT circuit can be used to learn the causal relationship between them using some causal discovery algorithms such as PC algorithm.

TABLE I
SIMULATION MODEL PARAMETERS

Parameters	Value
R_1	200 KΩ
R_2	100 KΩ
R_3	30 KΩ
R_4	22 KΩ
R_5	10 KΩ
R_6	5 KΩ
R_7	4.7 KΩ
V_{cc}	12 V

Parameters	Mean	Standard Deviation
T_1	50°C	6°C
T_2	50°C	5.6°C
T_3	50°C	5.3°C
T_4	50°C	5°C
T_5	50°C	5.5∘C
T_6	50°C	4.44°C
T_7	50°C	4.1°C
T_8	50°C	2.6°C
T_9	50°C	5.5°C
T_{10}	50°C	4.2°C
T_{11}	50°C	4.3°C

V. RESULTS AND DISCUSSION

This section presents the process of data generation using spice simulation, causal discovery with the generated data, and circuit diagnosis using causal structure of the network.

A. Spice Simulation and Data Generation

A direct coupled BJT circuit consisting of eleven 2N2222 *npn* BJTs [20] interconnected as shown in Fig. 3 was simulated in *LTspice* [21] for data generation. The circuit parameters of the simulation model are listed in Table I where T_n corresponds to the temperature of BJT Q_n. During the simulation the temperatures of the transistors were varied around a mean value and the DC operating point voltages and currents were measured at each temperature. The measured currents and voltages are annotated in Fig. 3, the currents were measured in *nA* scale and the voltages were measured in μV scale. Each of the temperature variables of the transistors were considered to be an independent Gaussian random variable with the same mean value but different standard deviation as listed in Table I. From the simulation, a data set consisting of $30,000$ data points in each variable was generated, which was further used for causal discovery.

B. Causal Search and DAG Identification

The generated data set was used to perform two separate causal search process; first, considering $\{I_1, I_2, I_3, I_4, I_5, I_6, I_7\}$ as the variables, and the second causal search considering $\{V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{C5}, V_{C6}, V_{C7}\}$ as the variables. Both of the search process was performed using the *PC algorithm* in *Tetrad* [22]. The Fisher Z-test [17] with a threshold of 0.01 was used for testing conditional independence of the variables in the data sets. The results obtained from Tetrad are depicted in Fig. 4. It can be observed that the generated DAG in both the cases come out to be the same as described below. A close inspection of the simulation schematic in Fig. 3 along with the DAGs in Fig. 4 reveals that the DAGs are in agreement with the layout of the circuit, i.e. the DAGs represent the causal structure one would expect considering the BJTs to be causal devices. This leads to some important implications for circuit diagnosis as described next.

C. Circuit Diagnosis Using DAG

Since the generated DAGs closely represent the actual construction and signal flow in the BJT circuit, the DAGs can be used to perform various kinds of analyses of the circuit with the help of various notions of causal inference, such as *Front Door Criteria, Back Door Criteria,* and *Markov Blankets* [15], [17]. One such application is fault diagnosis. An example case of fault diagnosis for the circuit considered here is discussed.

Consider V_{C7} to be the output and V_{B1}, V_{B2} to be the inputs of the circuit in Fig. 3. The inputs are considered to be sinusoidal voltages with 128 mV of peak to peak amplitude, 770 mV of DC offset, and a frequency of 5 KHz. Assume that a deviation of the output from expected result has occurred as shown in Fig. 5(a) due to failure of BJT Q_7 which has caused an open circuit fault, but these specific fault conditions are unknown to the user. The user is provided with the DAG representation of the circuit as in Fig. 4(b). Under such conditions, the user may develop test strategies with the help of the DAG of the network and standard causal inference notions to optimize number of required test, sensors etc.

A strategy of successive Markovian parent identification can be used to uncover faults. Markovian parents of a node $\bar{v} \in V$ is defined as the smallest set of nodes $\overline{\Pi} \in V$ such that $(\bar{v} \perp\!\!\!\perp V \setminus (\bar{v} \cup de(\bar{v})) | \overline{\Pi})$ i.e. given $\overline{\Pi}$, $\bar{v}$ is independent of its non-descendants [16]. From the DAG of Fig. 4(b) it can be observed that $dsep(V_{C7}, \{V_{C2}, V_{C3}, V_{C6}\}, \{V_{C1}, V_{C4}, V_{C5}\})$ holds which implies that under the assumption that the graph is faithful to the data, $(V_{C7} \perp\!\!\!\perp \{V_{C1}, V_{C4}, V_{C5}\} | \{V_{C2}, V_{C3}, V_{C6}\})$ holds i.e. $\{V_{C2}, V_{C3}, V_{C6}\}$ are Markovian parents of V_{C7}. Voltage measurement at these nodes reveal that the measured value of V_{C2}, V_{C3} are as expected as shown in Fig. 5(b) and Fig. 5(c), where as, the measured value of V_{C6} is erroneous as shown in Fig. 5(d). This implies that under the assumption that only one fault has occurred, the fault must be somewhere among the ancestors of V_{C6} and itself. As a logical next step V_{C5} is identified as the Markovian parent of V_{C6}, since $dsep(V_{C6}, V_{C5}, \{V_{C1}, V_{C2}, V_{C3}, V_{C4}\})$ holds. Again, measurement shows that measured value of V_{C5} is erroneous as in Fig. 5(e). Which again implies that the fault must be somewhere among its ancestors and itself. We now identify V_{C4} as the Markovian parent of V_{C5} using d-separation on the DAG of Fig. 4(b) and observe that measurement at V_{C4} is as expected as shown in Fig. 5(f). Which implies that there is no fault among its ancestors. Hence, the fault must somewhere between the node V_{C4} and V_{C5} which corresponds to the region pointed out by dotted red square in Fig 3. Thus, using only 5 tests it is possible to identify the faulty region, which is a significant improvement over traditional methods.

D. Discussion

It is to be noted that, although this article only presents the topology identification and fault diagnosis method for NPN BJT network, preliminary experimental results show that the method is equally applicable to PNP BJT, N-channel MOSFET, and P-channel MOSFET networks as well. Due to space limitations these results are not presented here.

VI. CONCLUSION AND FUTURE WORK

This study has shown that BJTs can be considered to be causal devices. It has been corroborated that the current and

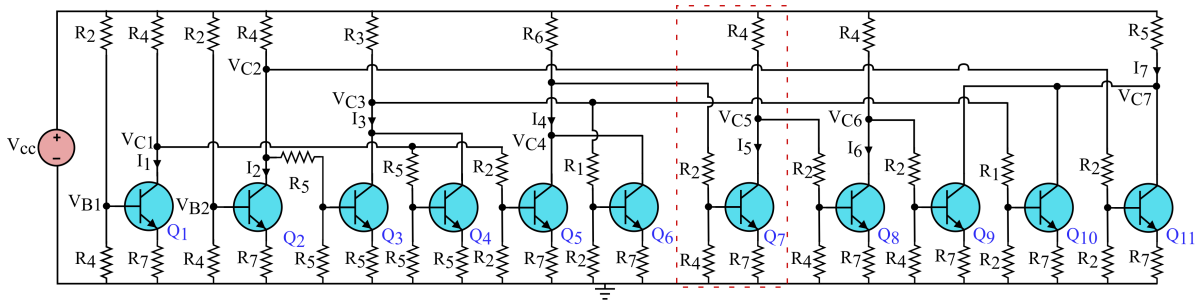

Fig. 3. Simulation Schematic

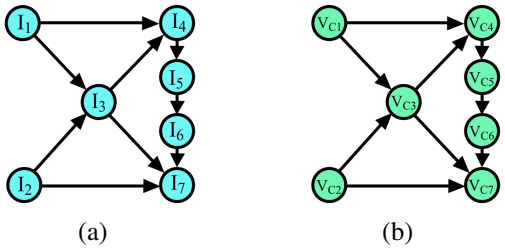

Fig. 4. Identified DAGs (a) Considering $\{I_1, I_2, I_3, I_4, I_5, I_6, I_7\}$ as the variables (b) Considering $\{V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{C5}, V_{C6}, V_{C7}\}$ as the variables

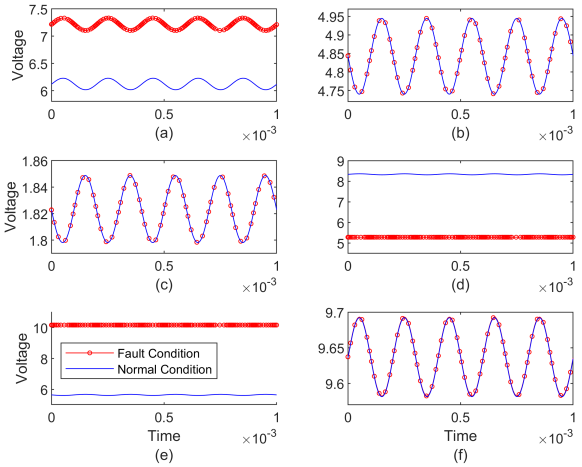

Fig. 5. Measured collector voltages under normal and fault conditions (a) V_{C7} (b) V_{C2} (c) V_{C3} (d) V_{C6} (e) V_{C5} (f) V_{C4}

voltage equations of a direct coupled BJT amplifier can be posed as SEMs and traditional causal discovery methods can be used on a BJT circuit to identify the causal structure of the network and construct a DAG representation. It was also demonstrated that the constructed DAG can further be used for fault diagnosis.

As part of the future work, development of similar methods for electronic circuits containing dynamics and feedback loops is under progress. Development and analysis of other topology informed fault diagnosis algorithms are underway. Application of the topology identification method to circuits containing uncertainties and noisy elements is also part of future endeavours.

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