2024 IEEE 63rd Conference on Decision and Control (CDC)
December 16-19, 2024. MiCo, Milan, Italy

Optimal Space Vector Modulation for Enhancing Reliability of the DC-Link Capacitor in a 2-Level Converter

Lars Bartels[2], Amin Rezaeizadeh[1], Florian Dörfler[2] and Silvia Mastellone[1]

***Abstract*— In power conversion applications, the DC-link capacitor is a critical component prone to degradation and its reliability affects the whole converter lifespan. Two-levels converters are commonly operated using pulse patterns designed according to conventional modulation schemes to generate a desired AC voltage. The effect of the switching on the DC-link capacitor current is not considered in the planned pulse pattern. This work proposes an alternative modulation strategy where the patterns are optimized to minimize the RMS current and thus reduce the degradation effect of current ripples on the capacitor. A comparative performance analysis of the reliability-based modulation scheme with respect to the standard practice is carried out based on simulation. The analysis results demonstrate that the proposed method generates the desired voltage output with low levels of harmonic distortion, while significantly decreasing RMS current values and thus enhancing capacitor lifetime.**

I. Introduction

Power electronic converters enable power control and adaptation for a wide spectrum of process needs at good energy efficiency levels. The ubiquitous employment of power converters in all energy, industry and mobility sectors led to increased research attention on various modulation techniques [1]–[6] to optimally operate those devices. Modulation techniques generate switching patterns to control the output voltage of a converter. The inherent discrete nature of these pulses however, introduces undesired harmonic content in both the converter output and the DC-link currents.

The capacitor connected to the DC side of the converter as in Fig. 1, is referred to as DC-link and is typically sized to reduce the voltage ripples and provide sufficient energy storage for transient operations [7, 8]. The Aluminum Electrolytic Capacitors (Al-Caps), widely employed in various power electronic applications [7], are the components with highest failure rate [9, 10] and limited lifespan [11, 12]. The main factor contributing to the degradation of electrolytic capacitors is electrolyte evaporation and electro-chemical reactions, which are influenced by electro-thermal stresses caused by temperature and current ripples. Additionally, high levels of ripple currents increase the power losses in the Equivalent Series Resistor (ESR) of the capacitor, those lead to an increased hot-spot temperature and further accelerate the aging process [12, 13].

*This work was supported by NCCR Automation and SNSF

[1]Amin Rezaeizadeh and Silvia Mastellone are with the Institute of Electric Power Systems, University of Applied Science Northwest Switzerland, Windisch-Brugg, Switzerland. amin.rezaeizadeh@fhnw.ch, silvia.mastellone@fhnw.ch

[2] Lars Bartels and Florian Dörfler are with the Automatic Control Lab (IfA) at ETH Zürich, Switzerland. dorfler@ethz.ch

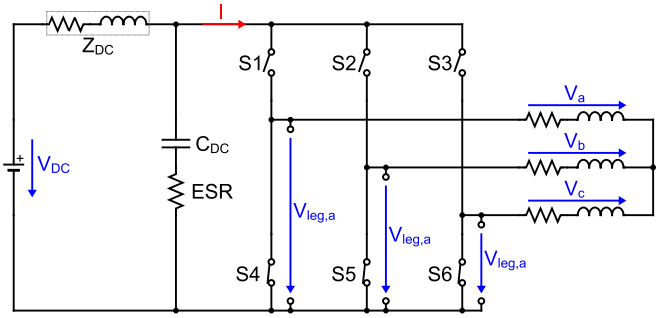

Fig. 1. Schematic diagram of a 2-level power conversion system

Increasing the converter switching frequency reduces the current harmonics and therefore the heat generated in the capacitor. On the other hand, it also leads to higher switching losses in the power semiconductors. To optimize the overall system efficiency and reliability, it is necessary to minimize both the current harmonics and the switching losses. To reduce harmonic distortion in the output of the converter, optimized pulse patterns (OPPs) [6, 14]–[17] are computed offline and applied as switching strategy. However, these OPP methods do not directly minimize the stress on DC-link capacitors. The main idea of this work is controlling the switching patterns to reduce current ripples and the associated stress factors, thus contributing to extend the lifetime of the capacitor [18]. Other less standard modulation methods [19]–[25], rely on heuristic approaches to reduce the DC-link capacitor current. In [26], the authors developed a look up table based on a mathematical optimization problem with the objective of minimizing the RMS value of the current in the DC-link. The problem is then solved by the `fmincon` function in MATLAB.

In this work, to address the reduction of heat generated in the DC-link capacitor, we rely on the relation between thermal losses and current RMS value, i.e. $P_{loss} = ESR \times I^2_{RMS}$, and choose the RMS value of the DC-link current as the optimization criterion. We formulate the current RMS minimization problem in a convex optimization framework based on SVM technique, while considering minimal switching loss patterns. Specifically, we propose two different methods. In the first method, a binary optimization problem is formulated to determine the optimal pulse patterns such that the RMS value of the DC link current is minimized. In the second method, a linear optimization problem (LP) is proposed where the optimal dwell times of the space vectors is determined, and the vectors are selected to achieve minimum switching losses.

TABLE I
SPACE VECTORS WITH CORRESPONDING STATE

Space Vector	Magnitude	Angle	$\mathbf{S_a}$	$\mathbf{S_b}$	$\mathbf{S_c}$
V_0	0		0	0	0
V_1	$2V_{DC}/3$	0°	1	0	0
V_2	$2V_{DC}/3$	60°	1	1	0
V_3	$2V_{DC}/3$	120°	0	1	0
V_4	$2V_{DC}/3$	180°	0	1	1
V_5	$2V_{DC}/3$	240°	0	0	1
V_6	$2V_{DC}/3$	300°	1	0	1
V_7	0		1	1	1

The rest of this paper is organized as follows. In section II, the standard modulation technique as well as the capacitor lifetime model are described. Section III introduces the optimization-based space vector modulation algorithms. The simulation results and the discussion are given in section IV, followed by concluding remarks.

II. PROBLEM DEFINITION

A. System Description

A 2-level converter consists of six power semiconductor switches arranged in three pairs, which each form a leg corresponding to one phase of the three-phase AC output. The schematic of a 2-level converter system, composed of a DC-link capacitor, power converter, and inductive load is depicted in Fig. 1. To prevent short circuits, the lower switch of a pair is required to always be in the opposite state from its upper switch. The state of a leg S_a, S_b, and S_c is hence binary, defined to be 1 if the upper switch is on and 0 otherwise.

Given a DC input voltage V_{DC}, the voltage vector at the output of the 2-level converter is given by

$$V = \frac{2}{3} V_{DC}(S_a + aS_b + a^2 S_c), \tag{1}$$

where $a = e^{j\frac{2\pi}{3}}$.

Since $S_a, S_b, S_c \in \{0, 1\}$ are all binary, V can take 8 discrete values, six of which are equally spaced around the origin on the unit circle in the complex plane, while V equals zero for the two cases where all legs have the same state 0 or 1. The eight resulting vectors V are called space vectors and are numbered according to Table I.

B. Space Vector Modulation

Space vector modulation (SVM) is a standard modulation technique used to define the switching pattern to obtain desired output waveforms with high efficiency and low harmonic distortion [27]. Whereas conventional pulse width modulation (PWM) methods work by switching between scalar voltage values, SVM uses a similar idea for the two-dimensional space vectors. Assume the converter is supposed to output a desired voltage V^* which can be decomposed as a weighted average of the space vectors V_i. SVM determines for how long each space vector should be active over the duration of a switching period T_{sw} such that the average voltage output over time, $\bar{V}$, approximates the desired voltage

$$V^* \approx \bar{V} = \frac{1}{T_{sw}} \sum_{i=0}^{7} T_i V_i \quad \text{with} \sum_{i=0}^{7} T_i = T_{sw}. \tag{2}$$

Note that (2) is not a well-posed problem since generally multiple combinations of space vectors are possible to reach V^*. While conventional SVM schemes compute a switching pattern by following some predefined rules on which space vectors are active and in what order they are applied, this additional degree of freedom can be exploited to optimize the operation according to additional desired criteria.

C. DC-Link Capacitor Lifetime Model

The equivalent series resistance (ESR) of a capacitor determines the power loss resulting from a given RMS capacitor current. This power has to be dissipated as heat and thus leads to a local hot spot temperature T_h. To calculate this temperature, let T_a be the ambient temperature and R_{ha} the thermal resistance between the hot spot and ambient. [12]

$$T_h = T_a + R_{ha} \times P_{loss} = T_a + R_{ha} \times ESR \times I_{RMS}^2 \tag{3}$$

The hot spot temperature T_h in combination with the operating voltage V allows an estimation of the capacitor lifetime L based on a rated lifetime L_0 at test voltage V_0 and test temperature T_0. The lifetime model is given as follows [7]

$$L = L_0 \left(\frac{V}{V_0}\right)^{-n} \exp\left(\frac{E_a}{K_B}\left(\frac{1}{T_h} - \frac{1}{T_0}\right)\right), \tag{4}$$

where $K_B = 8.62 \cdot 10^{-5}\,\mathrm{eV/K}$ is the Boltzmann constant and the activation energy E_a and n are hardware-dependent parameters that have to be determined.

As can be inferred from (3) and (4), the expected capacitor lifetime decreases for high capacitor current RMS values. The lifetime of the system can thus be increased by controlling the 2-level inverter in such a way that the resulting RMS current through the capacitor is minimized.

III. OPTIMIZATION-BASED MODULATION

To design a switching pattern that produces a low RMS current over the entire cycle, we consider each switching period separately and want to find optimal switching patterns that approximate the instantaneous desired complex voltage vector, and produce minimal RMS current within the considered switching period. If a switching period is chosen to be sufficiently small, then one can assume that the phase currents I_a, I_b, and I_c determined by the load on the output remain approximately constant over its duration and fluctuations in the total current I are hence only caused by the switching pattern. Further, we assume that the capacitor current is the AC component of I such that minimizing the RMS capacitor current is equivalent to minimizing the RMS value of I. Since the RMS value of the current over a full cycle is a strictly monotonically increasing function of the RMS currents of all the individual switching periods, this approach is guaranteed to lead to a lower overall RMS current than any other method using the same switching periods under the stated assumptions.

A. Optimization in the Time Domain

To optimize over the state of the converter as a function of time, we discretize a switching period into N time steps and then define $S_a, S_b, S_c \in \{0,1\}^N$ as optimization variables. Given the phase currents, the total current I over time can then be expressed in vector form as a linear combination of the optimization variables and its RMS value is given as

$$I_{RMS} = \frac{1}{\sqrt{N}}\|I\|_2 = \frac{1}{\sqrt{N}}\|S_a I_a + S_b I_b + S_c I_c\|_2. \quad (5)$$

Due to the discretization effect, the average voltage can no longer be assumed to outright equal the desired voltage. Instead, we introduce a soft constraint that requires the absolute difference between the desired and average voltage not to exceed some defined limit $\eta \geq 0$. The voltage error tolerance η is an important design parameter that can be chosen a priori or can be defined as an optimization variable and included in the cost function to penalize large values.

$$\left|V^* - \bar{V}\right| = \left|V^* - \frac{2}{3}V_{DC}\left(\bar{S}_a + a\bar{S}_b + a^2\bar{S}_c\right)\right| \leq \eta. \quad (6)$$

Additionally, to prevent over switching, which would lead to increased power losses, we introduce an additional set of constraints that require each leg to be switched on and off at most once per switching period. This can be enforced as a constraint on the difference between the state vector and state vector shifted by one position:

$$\left\|S_i - \begin{bmatrix} S_i^{[2:N]} & S_i^{[1]} \end{bmatrix}\right\|_1 \leq 2 \quad \text{for } i \in \{a,b,c\}. \quad (7)$$

Using the resulting RMS current as an objective function and requiring satisfaction of the voltage and switching constraints leads to the following constrained optimal control problem:

$$\begin{aligned} \min_{S_a,S_b,S_c\in\{0,1\}^N} & \|S_a I_a + S_b I_b + S_c I_c\|_2 \\ \text{subj. to } & \left|V^* - \frac{2}{3}V_{DC}\left(\bar{S}_a + a\bar{S}_b + a^2\bar{S}_c\right)\right| \leq \eta \\ & \left\|S_i - \begin{bmatrix} S_i^{[2:N]} & S_i^{[1]} \end{bmatrix}\right\|_1 \leq 2 \end{aligned} \quad (8)$$

Since the leg states are inherently constrained to be binary, (8) is a non-convex problem. A feasible solution satisfying the constraints can be found by using iterative methods as described in [28], but they only converge to a local optimum which may not be a good solution. [26] aims to solve a similar problem by initializing the search with a starting point near the global optimum.

B. Optimization in the Space Vector Domain

To prevent the practical issues caused by the binary constraint in (8), we propose a space vector modulation approach. Since a space vector captures the entire state of the inverter and the resulting RMS current is independent of the order in which different space vectors are applied, one can view the set of space vectors as the domain and optimize over the time T_i of how long any space vector V_i should be active. Thus, instead of dividing a switching period into N time steps, it is divided into eight sections of variable length corresponding to the space vectors. Both the RMS current and the voltage constraint can easily be reformulated as functions of the space vector on-times T_i:

$$\begin{aligned} T^* = \arg\min_{T_i\geq 0} & \sum_{i=0}^{7} T_i I_i^2 \\ \text{subj. to } & \sum_{i=0}^{7} T_i = T_{sw} \\ & \left|V^* - \frac{1}{T_{sw}}\sum_{i=0}^{7} T_i V_i\right| \leq \eta \end{aligned} \quad (9)$$

The solution of the optimization problem (9) is not an actual switching pattern but rather a property that an optimal switching pattern should fulfill. Hence, such a switching pattern has to be computed after solving (9). Therefore, the optimal T^* must be rounded to comply with a chosen discretization and the order in which the space vectors are applied has to be decided. This task can be formulated as a shortest path problem to minimize the switching losses resulting from applying the pattern. For this, interpret the space vectors that are active according to T^* as nodes and set the distance between two nodes to equal the number of switches necessary to flip between the space vectors. Then, find the shortest distance to visit all nodes and return to starting node. This problem is known as the symmetric traveling salesman shortest path problem and there exist efficient algorithms to solve it, especially for this case with only eight nodes, [29].

C. Optimization in SV Domain with Limited Switching

If we want to strictly limit switching, the optimization problem (9) can be modified slightly to restrict the set of space vectors used in the optimization in such a way that one leg is guaranteed to remain in a constant state during the switching period. Three neighboring space vectors always have one leg which is in the same state for all three of them. If this leg is in state 0, then also admit to use the zero space vector V_0, otherwise use the zero space vector V_7. With this constraint, there are always two possible combinations of four admissible space vectors. Let the sets $\mathcal{I}_1$ and $\mathcal{I}_2$ contain the respective indices of these allowed space vectors that depend on the desired. For example, if $0° \leq \angle V^* < 60°$, we have $\mathcal{I}_1 = \{0,1,2,3\}$ and $\mathcal{I}_2 = \{1,2,6,7\}$.

For each switching period, two convex optimization problems analogous to (9) are solved for $\mathcal{I}_1$ and $\mathcal{I}_2$, and the solution with minimum RMS current is selected. With the additional constraint, it is easy to arrange the four active space vectors in such a way that only four switches are required at most. In theory, this approach may lead to a better solution in terms of RMS current no longer being feasible, but simulations show this is not a big issue in practice.

IV. Simulation Result

A. Parameter Values and Methods

We consider the exemplary task of inverting a 700 V DC voltage into a three-phase sinusoidal AC voltage at a

TABLE II

DEFAULT PARAMETER VALUES IN SIMULATIONS

Parameter	Symbol	Value
DC input voltage	V_{DC}	700 V
AC frequency	ω_0	50 Hz
Desired AC amplitude	$\lvert V^* \rvert$	300 V
Current phase shift	ϕ	0°
Low-pass filter resistance	R	5 Ω
Low-pass filter inductance	L	5 mH
Low-pass filter capacitance	C	400 µF
Voltage error tolerance	η	$0.01 \times \frac{2}{3} V_{DC}$
Switching period	T_{sw}	100 µs
Resolution of discretization	N	40

frequency of 50 Hz with an amplitude of 325 V. We assume that the resulting phase currents can be approximated as a sine wave of the same frequency ω_0 and some phase shift ϕ. The amplitude of the current is normalized to 1 since it does not influence the optimal switching pattern but only scales the optimal value of the objective. An RLC low-pass filter is applied to the raw output voltage to eliminate the high frequencies caused by switching and produce a sinusoidal AC voltage. Unless stated otherwise, all results are obtained in simulations with the default parameter values listed in table II.

To provide a baseline to compare against, we consider software-determined and hardware-determined switching patterns from a standard space vector modulation scheme presented in [30]. These reference patterns are abbreviated as "SVPWM P1" and "SVPWM P2" respectively. They only focus on producing the desired output and do not take into account the resulting RMS current.

Next, we use the alternating direction method (ADM) from [28] to solve the binary optimal control problem (8). This approach is named "Binary Iteration" in the following plots.

Finally, we perform two optimizations in the space vector domain. The first method solves the unrestricted optimization problem (9) and then computes a switching pattern from the optimal T^* as a shortest path problem to minimize switching losses. The second method instead restricts the set of admissible space vectors to limit switching losses as described in section III-C. Let these respective approaches be called "Shortest Path" and "Limited Switching".

B. RMS Current and Switching Losses

With a fundamental frequency of 50 Hz and switching period of 100 µs, there are 200 distinct points per cycle at which a switching pattern has to be computed with the procedure given by the chosen method. Here, we consider these points individually and focus on how much RMS current and switching they cause locally. These values are plotted in Fig. 2 for all the considered control methods. Since a cycle is simply chaining together the resulting switching patterns, such a local comparison also allows us to draw conclusions about how well the methods perform over a larger time horizon.

It becomes clear that the binary iteration approach can not reliably converge toward a solution close to the global optimum. Meanwhile, the methods based on optimization in the space vector domain yield overall lower RMS current without a noticeably difference between them.

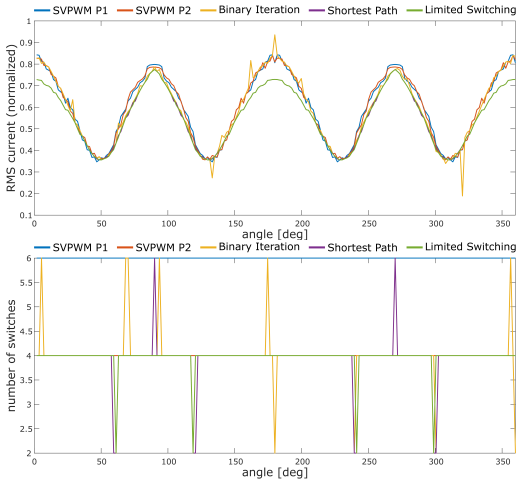

Fig. 2. RMS current and number of switches resulting from applying the computed computed switching patterns

It appears that enforcing a hard limit on the permitted switching may be unnecessary since excessive switching can be prevented by solving the shortest path problem from the solution of (9). For our exemplary parameter values, this even is more effective resulting in a total of 788 switches over a full cycle compared to 792 from solving the switching-constrained problem.

C. Capacitor Lifetime Analysis

To give an estimate of the achievable lifetime enhancement of the DC-link capacitor, we compare the "Shortest Path" approach with the "SVPWM P2", which we consider as a benchmark method. According to Fig. 6, we expect approximately 7.5% decrease in the RMS value of the capacitor current. Let I_{RMS} denote the baseline RMS capacitor current achieved by the standard space vector modulation scheme. From (3) the hot spot temperatures T_1 and T_2, corresponding to the SVPWM P2 and Shortest Path methods respectively, can be calculated. We assume the ambient temperature to be 20° C, the activation energy E_a of 0.94 eV, the ESR of 12 mΩ and the thermal resistance of 40 W/K are the same in both cases. Then, we use (4) to find an expression for the ratio between the lifetimes for both methods.

$$\frac{L_2}{L_1} = \exp\left(\frac{E_a}{K_B}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right) \tag{10}$$

Now, we can express the achieved improvement in expected lifetime as a function of the baseline RMS capacitor current, whose graph is plotted in Fig. 3. While its exact shape depends on the used hardware, it is clear that for a high enough baseline RMS current, the expected lifetime of the DC-link capacitor can be enhanced considerably.

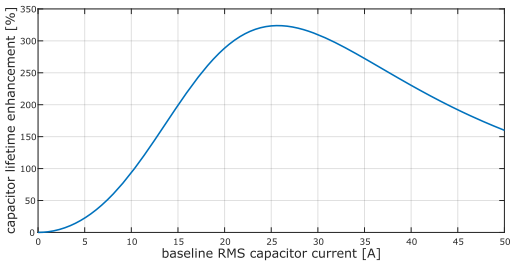

Fig. 3. Expected lifetime enhancement of DC-link capacitor plotted as a function of baseline RMS capacitor current

TABLE III
RMS CURRENT AND THD AT DEFAULT PARAMETER VALUES

Method	**RMS** (normalized)	**THD** (filtered)
SVPWM P1	0.6193	2.72%
SVPWM P2	0.6199	1.09%
Binary Iteration	0.6095	3.37%
Shortest Path	0.5769	2.04%
Limited Switching	0.5769	2.71%

D. Quality of Output Voltage

From visual inspection of the output voltage in the time and frequency domain, all methods seem to provide a decent sine wave after passing through the low-pass filter. The frequency spectra show a peak of around 325 V at the fundamental frequency of 50 Hz and some further spikes at the harmonics of the switching frequency at 10 kHz. The only outlier is the Fourier spectrum for the binary iteration solution, where the switching spikes look more chaotic.

For a quantitative comparison, consider the total harmonic distortion (THD) of the low-pass filtered output voltage. The THD values for all methods are listed in table III. The lowest THD comes with space vector modulation pattern #2 at 1.09%. For the binary iteration method, the disordered spikes in its Fourier spectrum cause the highest THD of 3.37%. The other approaches have a THD around 2% and 2.7% with the shortest path method being the best-performing of the optimization-based methods at 2.04%.

E. Dependence on Parameters

The phase currents are determined by the load attached to them. To account for different possible loads, we can vary the phase shift ϕ between voltage and current. Since this parameter is dictated by the electrical system, an optimization method that performs consistently well for all phase shifts is preferable. Fig. 6 shows that the space vector domain optimization methods clearly deliver the lowest RMS current across all current phase shift parameter values. On average this means around 7.5% decrease in RMS current compared to the conventional space vector modulation schemes. The THD shows some considerable fluctuations for all optimized patterns but generally remains in the range between 2% and 3%.

The voltage error tolerance η is a tunable parameter of the controller. Increasing η corresponds to relaxing the voltage

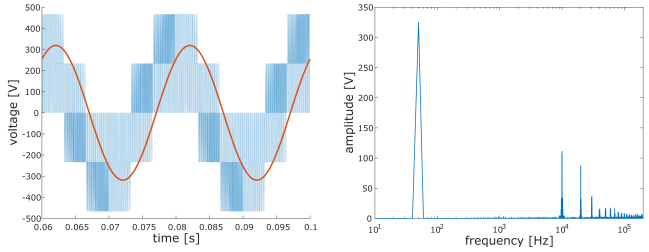

Fig. 4. Raw (blue) and filtered (orange) output voltage of phase a in time and frequency domain for method "SVPWM P2"

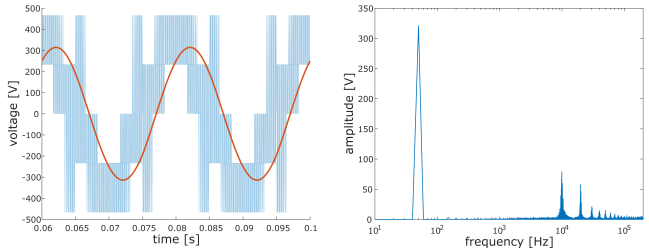

Fig. 5. Raw (blue) and filtered (orange) output voltage of phase a in time and frequency domain for method "Shortest Path"

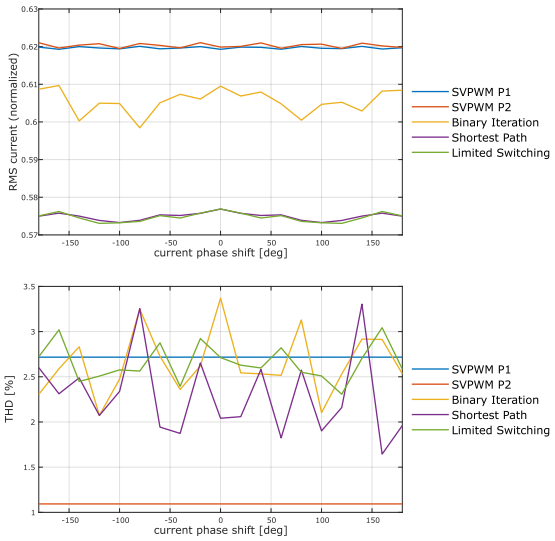

Fig. 6. RMS current and THD vs. current phase shift for all considered methods

constraint in the optimization problem. Simulations showed that both of the space vector domain optimization approaches can exploit the freedom given by relaxed voltage constraints to achieve an RMS current decrease that is close to linear. However, this supposed improvement comes at a significant cost in increased THD.

The switching frequency is another tuning parameter. Increasing the switching frequency inevitably leads to more switching losses but can also enable more precise tracking of the reference voltage causing a lower THD. The optimization problems themselves are not sensitive to such a modification and a significant discrepancy in resulting RMS current can thus not be observed. Also note that increasing the base

frequency ω_0 is computationally equivalent to decreasing the switching frequency. Hence, a change in ω_0 can be compensated by adjusting the switching period length accordingly.

Depending on what THD and switching losses are deemed acceptable for the respective application, the voltage error tolerance and switching frequency may themselves be subject to optimization as hyperparameters in order to meet the designated demands.

V. Conclusion

In this work we propose a modulation strategy to design switching patterns for a 2-level converter that achieve reduced RMS current in order to extend the expected lifetime of DC-link capacitors.

In particular, optimizing the patterns in the space vector domain proved to be a good strategy. It avoids the binary state constraints and results in a convex minimization problem. Furthermore, the set of active space vectors can be restricted to guarantee a limit on switching losses without sacrificing much performance.

The method performance is compared to those of the standard space vector modulation schemes. As demonstrated by the simulation results, the reliability-based modulation achieves a 7.5% reduction of the the RMS current with respect to the standard method. This leads to a significant enhancement of capacitor lifetime in various operating conditions while maintaining a high-quality voltage output with a low THD.

References

[1] J. Holtz, "Pulsewidth modulation-a survey," *IEEE Transactions on Industrial Electronics*, vol. 39, no. 5, pp. 410–420, 1992.

[2] G. Shiny and M. R. Baiju, "A fractal based space vector PWM scheme for general n-level inverters," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 847–854.

[3] K. S. Amitkumar and G. Narayanan, "Simplified implementation of space vector PWM strategies for a three level inverter," in *2012 IEEE 7th International Conference on Industrial and Information Systems (ICIIS)*, 2012, pp. 1–6.

[4] Y. Wang, X. Wen, F. Zhao, and X. Guo, "Selective harmonic elimination PWM technology applied in PMSMs," in *2012 IEEE Vehicle Power and Propulsion Conference*, 2012, pp. 92–97.

[5] P. R. Rakesh and G. Narayanan, "Analysis of sine-triangle and zero-sequence injection modulation schemes for split-phase induction motor drive," *IET Power Electronics*, vol. 9, no. 2, pp. 344–355, 2016.

[6] A. D. Birda, J. Reuss, and C. Hackl, "Synchronous optimal pulsewidth modulation with differently modulated waveform symmetry properties for feeding synchronous motor with high magnetic anisotropy," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1–P.10.

[7] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters-an overview," *IEEE Transactions on industry Applications*, vol. 50, no. 5, pp. 3569–3578, 2014.

[8] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 7, pp. 2950–2964, 2012.

[9] U. D. of Defense, Ed., *The Military Handbook for Reliability Prediction of Electronic Equipment MIL-HDBK-217F*. Defense Printing Service, 1995.

[10] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 3151–3157.

[11] W.-J. Lee and S.-K. Sul, "DC-link voltage stabilization for reduced DC-link capacitor inverter," *IEEE Transactions on industry applications*, vol. 50, no. 1, pp. 404–414, 2013.

[12] H. Wang, P. Davari, H. Wang, D. Kumar, F. Zare, and F. Blaabjerg, "Lifetime estimation of DC-link capacitors in adjustable speed drives under grid voltage unbalances," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4064–4078, 2018.

[13] Y. Liu, M. Zhu, M. Huang, and X. Zha, "An event-oriented reliability assessment for DC link capacitors in grid connected inverter with low voltage ride through operation," *Microelectronics Reliability*, vol. 138, p. 114768, 2022, 33rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis.

[14] A. Birth, T. Geyer, and H. du Toit Mouton, "Symmetry relaxation of three-level optimal pulse patterns for lower harmonic distortion," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1–P.10.

[15] G. S. Buja and G. B. Indri, "Optimal pulsewidth modulation for feeding AC motors," *IEEE Transactions on Industry Applications*, vol. IA-13, no. 1, pp. 38–44, 1977.

[16] A. K. Rathore, J. Holtz, and T. Boller, "Synchronous optimal pulsewidth modulation for low-switching-frequency control of medium-voltage multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2374–2381, 2010.

[17] A. Tripathi and G. Narayanan, "Optimal pulse width modulation of voltage-source inverter fed motor drives with relaxation of quarter wave symmetry condition," in *2014 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT)*, 2014, pp. 1–6.

[18] W. Sarjeant, "Capacitor fundamentals," in *Proceedings of the 19th Electrical Electronics Insulation Conference,*, 1989, pp. 1–51.

[19] S.-M. Kim, I. J. Won, J. Kim, and K.-B. Lee, "DC-link ripple current reduction method for three-level inverters with optimal switching pattern," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 12, pp. 9204–9214, 2018.

[20] X. Zhang, X. Wu, C. Geng, X. Ping, S. Chen, and H. Zhang, "An improved simplified PWM for three-level neutral point clamped inverter based on two-level common-mode voltage reduction PWM," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 11 143–11 154, 2020.

[21] Y.-J. Kim, S.-M. Kim, and K.-B. Lee, "Improving DC-link capacitor lifetime for three-level photovoltaic hybrid active NPC inverters in full modulation index range," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5250–5261, 2021.

[22] J.-H. Choi, U.-M. Choi, and F. Blaabjerg, "Hybrid pulse width modulation for improving reliability of DC-link capacitors of NPC inverter in photovoltaic systems," *IEEE Access*, vol. 12, pp. 18 752–18 763, 2024.

[23] A. Sangwongwanich, M. Novak, S. Sangwongwanich, and F. Blaabjerg, "Reliability of DC-link capacitors in three-level NPC inverters under different pwm methods," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1804–1811.

[24] X. Guo, D. Xu, J. M. Guerrero, and B. Wu, "Space vector modulation for DC-link current ripple reduction in back-to-back current-source converters for microgrid applications," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 10, pp. 6008–6013, 2015.

[25] A. Tcai, I. M. Alsofyani, I.-Y. Seo, and K.-B. Lee, "DC-link ripple reduction in a DPWM-based two-level VSI," *Energies*, vol. 11, no. 11, 2018.

[26] C. Grabher, "Optimized pulse patterns to minimize the current harmonic content in the DC-link of a two-level VSI," Master's thesis, Technische Universität München, 2019.

[27] P. Handley and J. Boys, "Space vector modulation: an engineering review," in *1990 Fourth International Conference on Power Electronics and Variable-Speed Drives (Conf. Publ. No. 324)*. IET, 1990, pp. 87–91.

[28] G. Yuan and B. Ghanem, "Binary optimization via mathematical programming with equilibrium constraints," *arXiv preprint arXiv:1608.04425*, 2016.

[29] K. L. Hoffman, M. Padberg, G. Rinaldi *et al.*, "Traveling salesman problem," *Encyclopedia of operations research and management science*, vol. 1, pp. 1573–1578, 2013.

[30] Z. Yu, "Space-vector PWM with TMS320C24x/F24x using hardware and software determined switching patterns," *Texas Instruments Application Report SPRA524*, pp. 24–28, 1999.